Voltage translation devices

A must for systems that employ logic families utilizing multiple power supply voltages

Introduction

Different classes of semiconductor logic employing different power supply voltages are often used on the same circuit board, and without some help, they can't communicate effectively. This is because each logic class uses different voltages to say "1" and "0".

For example VIH defines the minimum voltage that defines "1" to the input of a given logic class, and VOH stands for the minimum voltage that will appear as an output of "1" from members of the same class. For the 5V CMOS Logic Family, VOH is 4.44 V, and VIH is 3.5 volts. So within that class, an output specifying "1" is 0.94 V more than what is needed for an input to recognize as "1". No problem.

Members of the 2.5 V CMOS Logic Family are specified with a VOH of 2.0 V. But, as we just learned, an input of at least 3.5V is required by the 5V CMOS logic family for guaranteed recognition as a "1". The 5V CMOS device may interpret 2.0 volts as a "1", but, as defined, there's no guarantee. Big problem.

The bottom line is that for members of different logic classes, or topologies, to communicate effectively some translation, specifically voltage translation, will be necessary. The situation is illustrated in Figure 1.

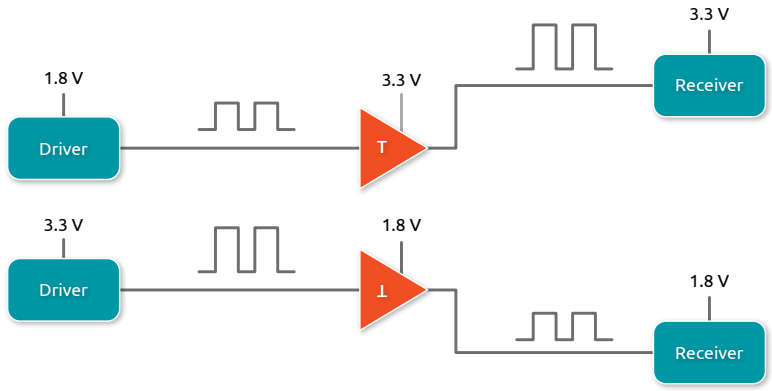

Figure 1. Some voltage translation is usually necessary between different logic classes or topologies

As we shall see, there are different types of voltage translation device topologies available to today's systems designers, each best suited to specific needs. These devices are typically available in industry standard logic families such as HC(T), AHC(T), LV, LVC, AUP, and AXP. Summary descriptions of these families and others mentioned in this article can be found here, on the third page of the document.

nexperia

Open drain topology

The open drain topology features an N-Channel FET in the voltage translation device, designated by T1 in Figure 2 below.

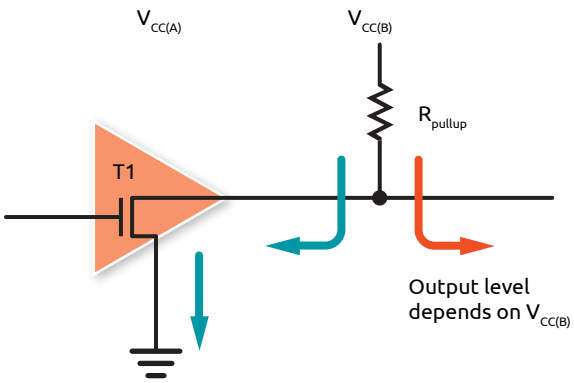

Figure 2. Open drain topology

One advantage of this topology is that the output voltage from T1 depends only on $V_{CC(B)}$. Also, inputs to the logic being fed by T1 can be wired OR, which will eliminate the need for additional components in some designs.

One disadvantage is relatively high power consumption caused by current flow through R_{pullup} from $V_{CC(B)}$ to ground. The RC time constant created by R_{pullup} and the input capacitance of the logic being fed by T1 may also be an issue, because it will cause a signal delay, which may be unacceptable in time critical applications.

Care must be taken in the choice of the pullup resistor. Among other concerns, the output edge slows as a function of increasing value.

Nexperia is offering open drain topology in their HC(T), AHC(T), LV, LVC, AUP, and AXP families.

Nexperia's 74LVC2G07 is an example of an open drain topology voltage translation device. Available in a variety of packages, members of this family can operate from supply voltages ranging from 1.65 V to 5.5 V, and are often used to couple logic devices operating at 3.3 V logic to those operating at 5 V logic levels.

Over-voltage tolerant topology

These devices can tolerate and successfully work with data inputs that are larger than their own V_{CC}'s. In the example below, a chip with a 3.3V V_{CC} is fed with 5V logic. The obvious advantage is simplicity of design and a lower chip count.

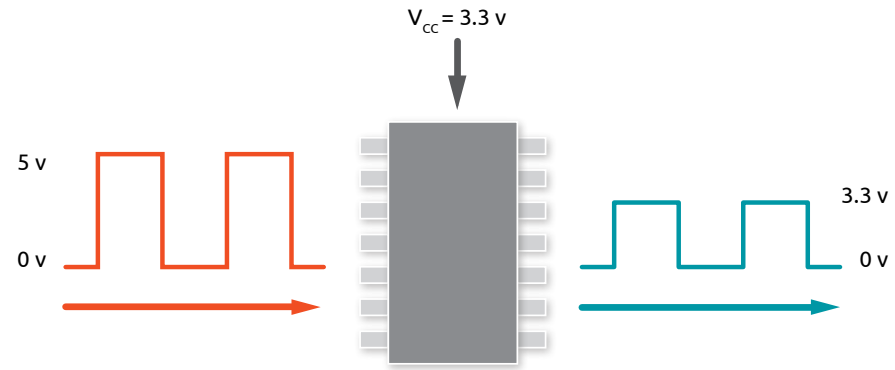

Figure 3. Over-voltage tolerant topology

One disadvantage here is that only down translation is possible; while 5V logic can feed a 3.3V chip, the reverse is not attainable with this topology. Another less obvious problem occurs if you have slow input logic signals (signals with slow rising and falling edges) as indicated in Figure 4 by the red graph. Because of the lower switching point, you'll get output of a different duty cycle than was presented at input. In our example below, the input duty cycle (red) is noticeably smaller than that of the output (blue). Of course, in certain situations, this is entirely unacceptable, precluding use of this type of device.

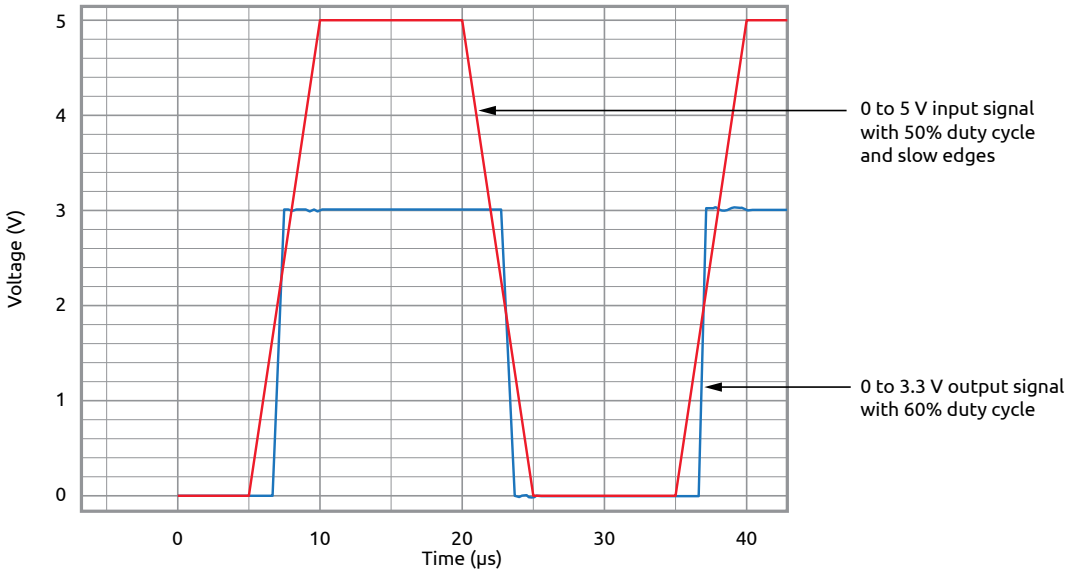

Figure 4. Comparison of input duty cycles between 3.3 V and 5.5 V

Nexperia is offering over-voltage tolerant topology in their AHC, ALVC, ALVT, AUP, AVC, AXP, LVC, LVT, and CBTLV(D) families.

The 74LVCV2G66GD is an example of a voltage translation device that is overvoltage tolerant. This device consumes very little operating power, and operate at voltages ranging from 2.3 V to 5.5V.

Single supply topology

For this topology, there is only one power supply, V_{CC}. If, for example, that V_{CC} is 3.3V, the device will be able to accept input logic levels from 1.8V to 3.3V. The logic output level for "high" will be 3.3V, reflecting the value of V_{CC}. A disadvantage here is that these chip are more power hungry than the dual supply topology devices that we next discuss. This topology provides up/down translation across multiple logic functions.

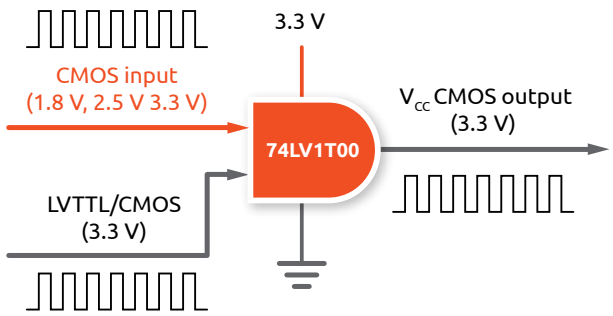

Figure 5. Single power supply translator

Nexperia is offering single supply translators in their LV, AUP families.

Dual supply topology

In the typical situation we describe here, there are two digital subsystems, one running with a V_{CC} of 1.2V, the other at 3V. Voltage translators of this type need to be provided both V_{CC}'s. Notice that they are bidirectional; they can transmit logic from the 1.2V subsystem to the 3V subsystem or traffic can be run the other way. A switching pin on the chip controls the directional flow, although some members of this chip topology have auto-sensing; they detect which direction is being presented with changing logic levels and accept that direction as the input.

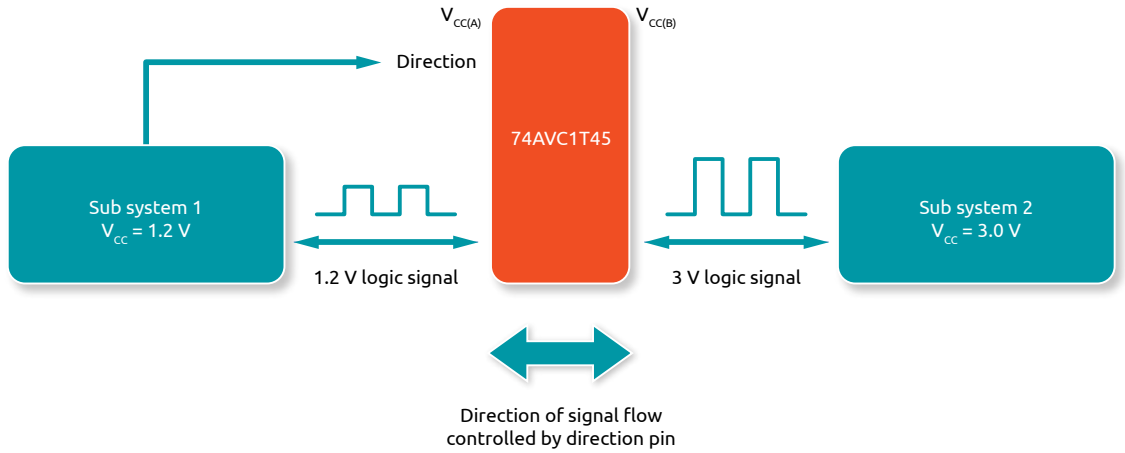

Figure 6. Dual supply topology

As previously mentioned, this topology is quite power-efficient. The bidirectionality can also be a boon to designers. Members of this topology are often used to service busses of 8 or 16 bits with one device.

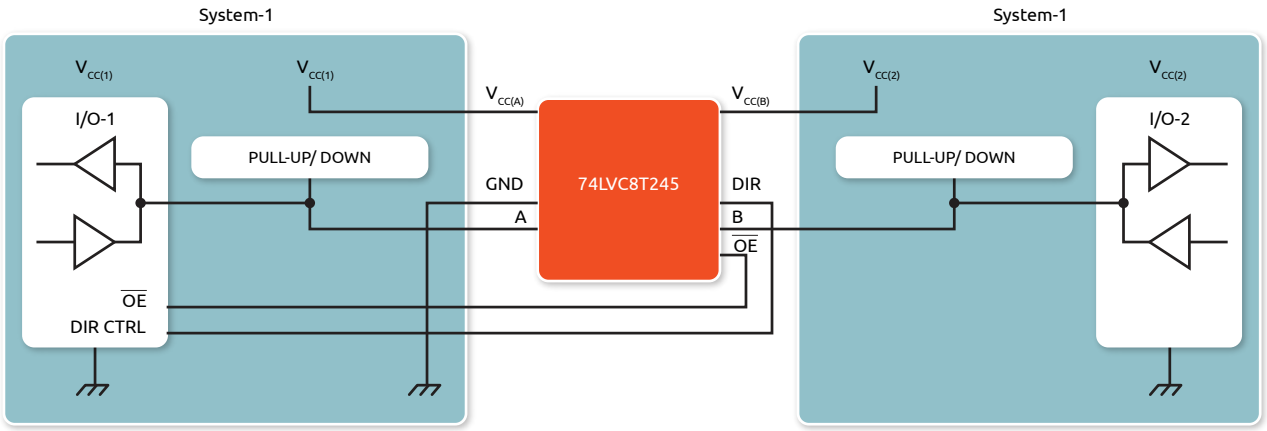

Figure 7. Typical bidirectional logic level-shifting application

Nexperia is offering dual-supply translators in their AVC, ALVC, AUP, LVC, and AXP families. The 74LVC8T245PW can operate from V_{CC}'s ranging from 1.2 V to 5.5 V, enabling the device to translate, in either direction, between any of the typical logic levels (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). For this device, translation direction is pin controlled, and isolation between the two busses can also be effected when need be, especially during power-down of the system.

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