Dealing with floating inputs in digital systems

In the normal operations of a digital system, the input to any digital device within is clearly defined — it is either one or zero. But, there are situations that are not entirely “normal”.

Consider first a situation of 8, 16, 32 or 64 inputs, arranged in a bus. Typically, any of a number of drivers may control this input bus. But, in some cases, none of the active drivers has been engaged by the overall system. Uncontrolled, the voltage present at the inputs are determined by random, unpredictable factors, not defined by the design of the overall system. That uncontrolled input is said to “float”.

Random events may unpredictably bring the floating input voltage up to a point that the device will interpret as a one, or down to the point that the device will interpret as a zero. Worse yet, the floating input may vary back and forth in an unpredictable manner, possible causing oscillation, which at the very least wastes system power and at worst renders the system inoperable.

The second situation occurs on power-up of the system. The design may require that the input to the bus be either one or zero. If the bus controlling the input to the digital devices is not otherwise defined at startup, it cannot be assumed that the input will be the one or the zero that is hoped for.

The first of these issues can be controlled by what is defined as bus-hold circuitry. The second situation can be controlled by either pull-up or pull-down resistors.

Bus-hold circuitry eliminates floating inputs

Figure 1 is a representation of the input to a CMOS digital component. If V1 is solidly one, the NMOS inverter buffer on the bottom switches on, and the PMOS inverter buffer on the top switches off. This latches the output to ground, or an output of digital zero. If V1 is solidly zero, the opposite happens, and the output is latched to V_{CC}, or digital one.

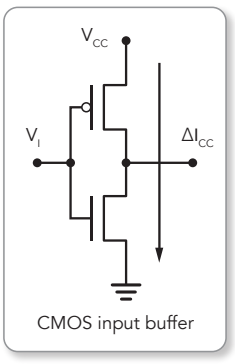

Figure 1

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The problems start when V1 floats — it isn't one or zero - and both the NMOS and PMOS inverter buffers operate in their linear ranges, allowing current I_{CC} to flow thru both inverters. The result is that the output isn't synched to either V_{CC} or Ground, one or zero. Thus, the output, too, floats, just like the input.

A way to get around this is employ a "bus hold" circuit that can latch in the last one or zero input presented to the devices input pin. Thus, even if the input would otherwise float, that input is held to its previous value. Here's what it looks like (Figure 2).

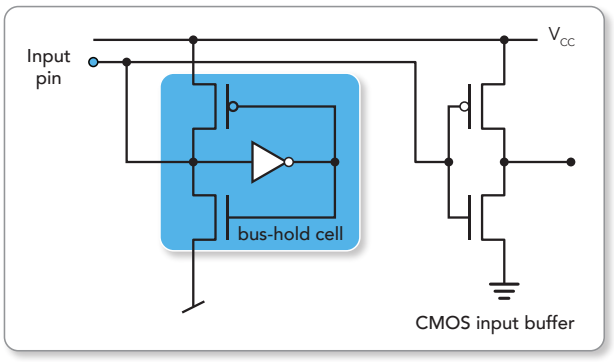

Figure 2

Does the blue section look familiar? Yes, the bus hold circuitry is, in its essence, a flip-flop. And, it requires enough current to switch states that random, floating signals applied to it will have no effect. Only a solid one or zero will cause it to switch. Thus, even when the input floats, the overall output stays at the value mandated by the last, solid input of one or zero.

Pull-up or pull-down resistors for a solid start up

But, the solution as described above may not always be enough. When a system first powers on, the system may require that the output of a device such as the one represented in Figure 1 must start off with a one or a zero. The input to the device may be floating, but of course, in this case the bus-hold circuitry has nothing to "remember", so there can be no help from that quarter. A similar situation may also exist when the devices is shut down.

The solution might either be a pull-up resistor from V_{CC} to enforce an input of one, or a pull-down resistor to enforce an input of zero.

Calculating resistor values

Let's take the case of a pull-up resistor. The formula used to calculate its value is:

$$R_{PULL\text{-}UP} = (V_{CC} - V_{TH}) / I_{BHLO}$$

V_{CC} is the value of the chips power supply. We will assume, for this example that the chip takes 3.0 V.

V_{TH} is a function of V_{IH}, the input voltage that the chip will always recognize as a one, and V_{IL}, the voltage that the chip will always recognize as zero:

$$V_{TH} = (V_{IH} + V_{IL}) / 2$$

If V_{IH} is 2.0 V and V_{IL} is 0.8 V

$$V_{IH} = (2.0 + 0.8) / 2$$
$$V_{IH} = 1.4V$$

I_{BHLO} This is a value that the designer can get from the Nexperia datasheet for the device. Let's assume 500 microamps, or 500 x 10^{-6} amps.

So, substituting values:

$R_{PULL\text{-}UP} = (V_{CC} - V_{TH}) / I_{BHLO}$

$R_{PULL\text{-}UP} = (3.0 - 1.4) / 500 \times 10^{-6}$

$R_{PULL\text{-}UP} = 1.6 / .5 \times 10^{-3} = 3200$ ohms

Pull-down resistor

For a pull-down resistor, the formula is:

$R_{PULL\text{-}DOWN} = (V_{TH}) / I_{BHLO})$

A similar calculation yields 2800 Ohms

Figure 3 shows a typical bus-hold characteristics and the effect of different pull-up resistors values. For values less than 8k there is no intersection of the load line with bus-hold line, so no issue in pulling up an initial low state input to high state. For larger resistor values the load line intersects the bus-hold line and this intersection point becomes the maximum voltage level to which the bus-hold is pulled from low, the input is never switching to high beyond this point.

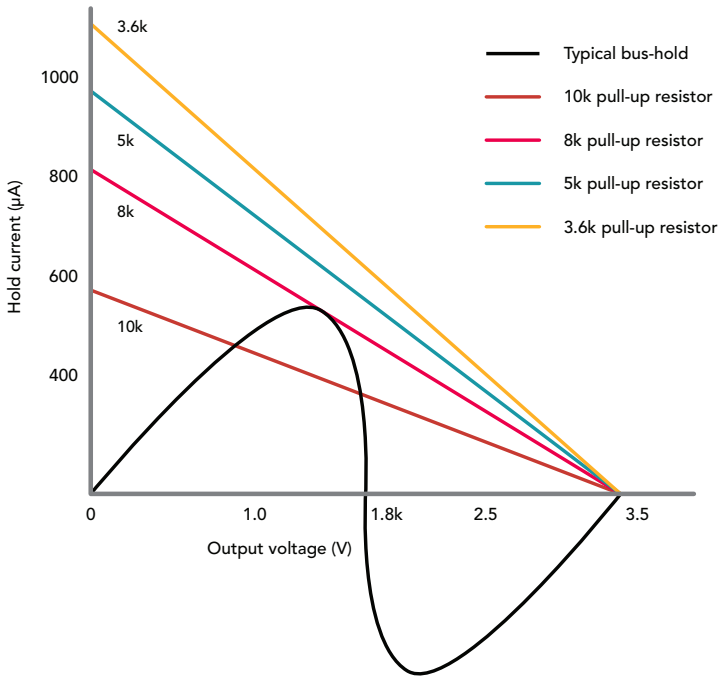

Figure 3

Problems inherent with pull-up and pull-down resistors

The input to the bus-hold circuitry, as well circuit board trace to the devices input form, what is, an effect, a capacitor. In series with the pull-up or pull-down resistor, an RC circuit is generated.

This has the potential to create problems. The input signal takes a finite amount of time to change the voltage on the input from either one to zero, or from zero to one. Thus, switching time is impacted. For this reason, the use of pull-up and pull-down resistors should be avoided if possible.

Availability of the bus-hold feature

The bus-hold feature is standard on all of Nexperia's LVT (Low Voltage Technology) and ALVT (Advanced Low-Voltage BiCMOS Technology) bus-interface products. This includes all 8-, 16-, and 32-bit buffers, inverters, drivers, flip-flops, latches/registered drivers, level shifters/translators, and transceivers.

On other Nexperia families, the bus-hold feature is indicated by an "H" in the product number. An example would be 74LVCH245 instead of 7474LVC245).

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